


Form 1449*	Atty. Docket No.: 303.389US2	Serial No. Unknown
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	Applicant: Leonard Forbes et al.	
	Filing Date: Herewith	Group: Unknown

U.S. PATENT DOCUMENTS

**Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
EL	4,051,354	09/27/1977	Choate, W.C.	235	312	07/03/75
EL	4,604,162	08/05/1986	Sobczak, Z.P.	156	657	12/23/85
EL	4,663,831	05/12/1987	Birrittella, M.S., et al.	29	576 E	10/08/85
EL	4,673,962	06/16/1987	Chatterjee, P.K., et al.	357	23.6	03/21/85
EL	4,761,768	08/02/1988	Turner, J.E., et al.	365	201	03/04/85
EL	4,766,569	08/23/1988	Turner, J.E., et al.	365	185	06/05/86
EL	4,906,590	03/06/1990	Kanetaki, Y., et al.	437	52	04/24/89
EL	4,920,065	04/24/1990	Chin, D., et al.	437	52	10/27/89
EL	4,958,318	09/18/1990	Harari, E.	365	149	07/08/88
EL	4,987,089	01/22/1991	Roberts	437	34	07/23/90
EL	5,001,526	03/19/1991	Gotou, H.	357	23.6	11/07/88
EL	5,006,909	04/09/1991	Kosa, Y.	357	23.6	10/30/89
EL	5,017,504	05/21/1991	Nishimura, et al.	437	40	04/21/89
EL	5,021,355	06/04/1991	Dhong, et al.	437	35	05/18/90
EL	5,028,977	07/02/1991	Kenneth, et al.	357	43	06/16/89
EL	5,057,896	10/15/1991	Gotou, H.	357	49	05/30/89
EL	5,072,269	12/10/1991	Hieda, K.	357	23.6	03/15/89
EL	5,102,817	04/07/1992	Chatterjee, P.K., et al.	437	47	11/26/90
EL	5,110,752	05/05/1992	Lu	437	47	07/10/91
EL	5,128,831	07/02/1992	Fox III, A., et al.			10/31/91
EL	5,156,987	10/20/1992	Sandhu, et al.	437	40	12/18/91
EL	5,177,028	01/05/1993	Manning	437	41	10/22/91
EL	5,177,576	01/05/1993	Kimura, S., et al.	257	71	05/06/91
EL	5,191,509	03/02/1993	Wen, D.	361	311	12/11/91
EL	5,202,278	04/13/1993	Mathews, et al.	437	47	09/10/91
EL	5,208,657	05/04/1993	Chatterjee, P.K., et al.	257	302	06/22/91
EL	5,216,266	06/01/1993	Ozaki, H.	257	302	04/09/91
EL	5,223,081	06/29/1993	Doan	156	628	07/03/91
EL	5,266,514	11/30/1993	Tuan, H., et al.	437	52	12/21/92
EL	5,292,676	03/08/1994	Manning	437	46	07/29/92
EL	5,316,962	05/31/1994	Matsuo, N., et al.	437	52	08/06/92
EL	5,320,880	06/14/1994	Sandhu, G.S., et al.	427	578	11/18/93
EL	5,327,380	07/05/1994	Kersh, III, D.V., et al.	365	195	02/08/91
EL	5,376,575	12/27/1994	Kim, J.S., et al.	437	52	09/24/92
EL	5,385,854	01/31/1995	Batra, et al.	437	41	07/15/93
EL	5,391,911	02/21/1995	Beyer, et al.	257	522	04/22/94
EL	5,392,245	02/21/1995	Manning	365	200	08/13/93
EL	5,393,704	02/28/1995	Huang, C.H., et al.	437	203	12/13/93

Examiner



Date Considered

11/21/00

*Substitute Disclosure Statement Form (PTO-1449)

**EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form 1449*	Atty. Docket No.: 303.389US2	Serial No. Unknown
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	Applicant: Leonard Forbes et al.	
	Filing Date: Herewith	Group: Unknown

U.S. PATENT DOCUMENTS

**Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
EL	5,396,093	03/07/1995	Lu	257	306	08/12/94
EL	5,409,563	04/25/1995	Cathey	156	643	02/26/93
EL	5,410,169	04/25/1995	Yamamoto, T., et al.	257	301	02/22/93
EL	5,414,287	05/09/1995	Hong, G.	257	316	04/25/94
EL	5,422,499	06/06/1995	Manning, M.	257	67	02/22/93
EL	5,427,972	06/27/1995	Shimizu, M., et al.	437	52	04/18/90
EL	5,432,739	07/11/1995	Pein, H.B.	365	185	06/17/94
EL	5,438,009	08/01/1995	Yang, M.-., et al.	437	52	04/02/93
EL	5,440,158	08/08/1995	Sung-Mu, H.	257	314	07/05/94
EL	5,445,986	08/29/1995	Hirota	437	60	09/01/94
EL	5,451,889	09/19/1995	Heim, B.B., et al.	326	81	03/14/94
EL	5,460,316	10/24/1995	Hefelee, H.L.	228	39	09/15/94
EL	5,460,988	10/24/1995	Hong, G.	437	43	04/25/94
EL	5,466,625	11/14/1995	Hsieh, C.M., et al.	437	52	11/22/94
EL	5,483,094	01/09/1996	Sharma, U., et al.	257	316	09/26/94
EL	5,483,487	01/09/1996	Sung-Mu, H.	365	185.33	04/24/95
EL	5,492,853	02/20/1996	Jeng, et al.	437	60	03/11/94
EL	5,495,441	02/27/1996	Hong, G.	365	185.01	05/18/94
EL	5,497,017	03/05/1996	Gonzales, /.	257	306	01/26/95
EL	5,502,629	03/26/1996	Ito, H., et al.	363	60	03/28/95
EL	5,504,357	04/02/1996	Kim, J.S., et al.	257	306	06/30/94
EL	5,508,219	04/16/1996	Bronner, G.B., et al.	437	52	06/05/95
EL	5,508,542	04/16/1996	Geiss, et al.	257	301	10/28/94
EL	5,519,236	05/21/1996	Ozaki, T.	257	302	06/27/94
EL	5,528,062	06/18/1996	Hsieh, et al.	257	298	06/17/92
EL	5,563,083	10/08/1996	Pein, H.B.	437	43	04/21/95
EL	5,574,299	11/12/1996	Kim, H.	257	296	06/29/95
EL	5,593,912	01/14/1997	Rajeevakumar, T.V.	437	52	10/06/94
EL	5,616,934	04/01/1997	Dennison, et al.	257	67	03/22/96
EL	5,640,342	06/17/1997	Gonzalez	365	156	11/20/95
EL	5,641,545	06/24/1997	Sandhu, G.S.	427	573	06/07/95
EL	5,644,540	07/01/1997	Manning	365	200	02/17/95
EL	5,646,900	07/08/1997	Tsukude, et al.	365	205	01/11/96
EL	5,691,230	11/25/1997	Forbes, L.	437	62	09/04/96
EL	5,705,415	01/06/1998	Orlowski, M.K., et al.	437	43	10/04/94
EL	5,760,434	06/02/1998	Zahurak, J.K., et al.	257	309	05/07/96
EL	5,789,967	08/04/1998	Katoh, Y.	327	408	04/01/96
EL	5,801,413	09/01/1998	Pan, P.	257	301	12/19/95

Examiner

Date Considered

*Substitute Disclosure Statement Form (PFD-1449)

**EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form 1449*	Atty. Docket No.: 303.389US2	Serial No. Unknown
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	Applicant: Leonard Forbes et al.	
	Filing Date: Herewith	Group: Unknown

U.S. PATENT DOCUMENTS

**Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
EL	5,821,796	10/13/1998	Yaklin, D., et al.	327	313	09/23/96
EL	5,852,375	12/22/1998	Byrne, T.G., et al.	327	108	02/07/97
EL	5,877,061	03/02/1999	Halle, S.D., et al.	438	386	02/25/97

FOREIGN PATENT DOCUMENTS

**Examiner Initial	Document Number	Date	Country	Class	Subclass	Translation Yes No
EL	363066963A	03/01/1988	Japan	257	305	

OTHER DOCUMENTS

(Including Author, Title, Date, Pertinent Pages, Etc.)

**Examiner Initial	
	Adler, E., et al., "The Evolution of IBM CMOS DRAM Technology", 167-188, (Jan./Mar., 1995)
	Asai, S., et al., "Technology Challenges for Integration Near and Below 0.1 micrometer", <u>Proceedings of the IEEE, 85</u> , Special Issue on Nanometer-Scale Science & Technology, 505-520, (Apr. 1997)
	Banerjee, S.K., et al., "Characterization of Trench Transistors for 3-D Memories", <u>1986 Symposium on VLSI Technology, Digest of Technical Papers</u> , San Diego, CA, 79-80, (May 28-30, 1986)
	Blalock, T.N., et al., "A High-Speed Sensing Scheme for 1T Dynamic RAM's Utilizing the Clamped Bit-Line Sense Amplifier", <u>IEEE Journal of Solid-State Circuits</u> , 27(4), pp. 618-624, (April 1992)
	Bomchil, G., et al., "Porous Silicon: The Material and its Applications in Silicon-On-Insulator Technologies", <u>Applied Surface Science</u> , 41/42, 604-613, (1989)
	Burnett, D., et al., "Implications of Fundamental Threshold Voltage Variations for High-Density SRAM and Logic Circuits", <u>1994 Symposium on VLSI Technology, Digest of Technical Papers</u> , Honolulu, HI, 15-16, (June 4-7, 1994)
	Burnett, D., et al., "Statistical Threshold-Voltage Variation and its Impact on Supply-Voltage Scaling", <u>Proceedings SPIE: Microelectronic Device and Multilevel Interconnection Technology</u> , 2636, 83-90, (1995)

Examiner 	Date Considered 11/21/00
---	-----------------------------

*Substitute Disclosure Statement Form (PTO-1449)

**EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form 1449*	Atty. Docket No.: 303.389US2	Serial No. Unknown
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	Applicant: Leonard Forbes et al.	
	Filing Date: Herewith	Group: Unknown

OTHER DOCUMENTS

**Examiner
Initial

(Including Author, Title, Date, Pertinent Pages, Etc.)

	Chen, M.J., et al., "Back-Gate Forward Bias Method for Low-Voltage CMOS Digital Circuits", <u>IEEE Transactions on Electron Devices</u> , 43, 904-909, (June 1986)
	Chen, M.J., et al., "Optimizing the Match in Weakly Inverted MOSFET's by Gated Lateral Bipolar Action", <u>IEEE Transactions on Electron Devices</u> , 43, 766-773, (May 1996)
	Chung, I.Y., et al., "A New SOI Inverter for Low Power Applications", <u>Proceedings of the 1996 IEEE International SOI Conference</u> , Sanibel Island, FL, 20-21, (Sep. 30-Oct. 3, 1996)
	De, V.K., et al., "Random MOSFET Parameter Fluctuation Limits to Gigascale Integration (GSI)", <u>1996 Symposium on VLSI Technology, Digest of Technical Papers</u> , Honolulu, HI, 198-199, (June 11-13, 1996)
	Denton, J.P., et al., "Fully Depleted Dual-Gated Thin-Film SOI P-MOSFET's Fabricated in SOI Islands with an Isolated Buried Polysilicon Backgate", <u>IEEE Electron Device Letters</u> , 17(11), 509-511, (Nov. 1996)
	Fong, Y., et al., "Oxides Grown on Textured Single-Crystal Silicon--Dependence on Process and Application in EEPROMs", <u>IEEE Transactions on Electron Devices</u> , 37(3), pp. 583-590, (March 1990)
	Forbes, L., et al., "Resonant Forward-Biased Guard-Ring Diodes for Suppression of Substrate Noise in Mixed-Mode CMOS Circuits", <u>Electronics Letters</u> , 31, 720-721, (April 1995)
	Foster, R., et al., "High Rate Low-Temperature Selective Tungsten", In: <u>Tungsten and Other Refractory Metals for VLSI Applications III</u> , V.A. Wells, ed., Materials Res. Soc., Pittsburgh, PA, 69-72, (1988)
	Fuse, T., et al., "A 0.5V 200MHz 1-Stage 32b ALU Using a Body Bias Controlled SOI Pass-Gate Logic", <u>1997 IEEE International Solid-State Circuits Conference, Digest of Technical Papers</u> , 286-287, (1997)
	Gong, S., et al., "Techniques for Reducing Switching Noise in High Speed Digital Systems", <u>Proceedings of the 8th Annual IEEE International ASIC Conference and Exhibit</u> , 21-24, (1995)

Examiner	Date Considered
----------	-----------------

*Substitute Disclosure Statement Form (PTO-1449)

**EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form 1449*	Atty. Docket No.: 303.389US2	Serial No. Unknown
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	Applicant: Leonard Forbes et al.	
	Filing Date: Herewith	Group: Unknown

OTHER DOCUMENTS

**Examiner
Initial

(Including Author, Title, Date, Pertinent Pages, Etc.)

	Hao, M.Y., et al., "Electrical Characteristics of Oxynitrides Grown on Textured Single-Crystal Silicon", <u>Appl. Phys. Lett.</u> , 60, 445-447, (Jan. 1992)
	Harada, M., et al., "Suppression of Threshold Voltage Variation in MTCMOS/SIMOX Circuit Operating Below 0.5 V", <u>1996 Symposium on VLSI Technology, Digest of Technical Papers</u> , Honolulu, HI, 96-97, (June 11-13, 1996)
	Heavens, O., <u>Optical Properties of Thin Solid Films</u> , Dover Pubs. Inc., New York, 167, (1965)
	Hisamoto, D., et al., "A New Stacked Cell Structure for Giga-Bit DRAMs using Vertical Ultra-Thin SOI (DELTA) MOSFETs", <u>1991 IEEE International Electron Devices Meeting, Technical Digest</u> , Washington, D.C., 959-961, (Dec. 8-11, 1991)
	Hodges, D.A., et al., "MOS Decoders", <u>In: Analysis and Design of Digital Integrated Circuits, 2nd Edition</u> , Section: 9.1.3, 354-357, (1988)
	Holman, W.T., et al., "A Compact Low Noise Operational Amplifier for a 1.2 Micrometer Digital CMOS Technology", <u>IEEE Journal of Solid-State Circuits</u> , 30, 710-714, (June 1995)
	Horie, H., et al., "Novel High Aspect Ratio Aluminum Plug for Logic/DRAM LSI's Using Polysilicon-Aluminum Substitute", <u>Technical Digest: IEEE International Electron Devices Meeting</u> , San Francisco, CA, 946-948, (1996)
	Hu, G., et al., "Will Flash Memory Replace Hard Disk Drive?", <u>1994 IEEE International Electron Device Meeting</u> , Panel Discussion, Session 24, Outline, 1 p., (Dec. 13, 1994)
	Huang, W.L., et al., "TFSOI Complementary BiCMOS Technology for Low Power Applications", <u>IEEE Transactions on Electron Devices</u> , 42, 506-512, (Mar. 1995)
	Jun, Y.K., et al., "The Fabrication and Electrical Properties of Modulated Stacked Capacitor for Advanced DRAM Applications", <u>IEEE Electron Device Letters</u> , 13, 430-432, (Aug. 1992)

Examiner	Date Considered
----------	-----------------

*Substitute Disclosure Statement Form (PTO-1449)

**EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form 1449*	Atty. Docket No.: 303.389US2	Serial No. Unknown
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	Applicant: Leonard Forbes et al.	
	Filing Date: Herewith	Group: Unknown

OTHER DOCUMENTS

**Examiner
Initial

(Including Author, Title, Date, Pertinent Pages, Etc.)

	Jung, T.S., et al., "A 117-mm ² 3.3-V Only 128-Mb Multilevel NAND Flash Memory for Mass Storage Applications", <u>IEEE Journal of Solid-State Circuits</u> , 31, 1575-1582, (Nov. 1996)
	Kang, H.K., et al., "Highly Manufacturable Process Technology for Reliable 256 Mbit and 1Gbit DRAMs", <u>IEEE International Electron Devices Meeting, Technical Digest</u> , San Francisco, CA, 635-638, (Dec. 11-14, 1994)
	Kim, Y.S., et al., "A Study on Pyrolysis DMEAA for Selective Deposition of Aluminum", In: <u>Advanced Metallization and Interconnect Systems for VLSI Applications in 1995</u> , R.C. Ellwanger, et al., (eds.), Materials Research Society, Pittsburgh, PA, 675-680, (1996)
	Kishimoto, T., et al., "Well Structure by High-Energy Boron Implantation for Soft-Error Reduction in Dynamic Random Access Memories (DRAMs)", <u>Japanese Journal of Applied Physics</u> , 34, 6899-6902, (Dec. 1995)
	Klaus, et al., "Atomic Layer Controlled Growth of SiO ₂ Films Using Binary Reaction Sequence Chemistry", <u>Applied Physics Lett.</u> 70(9), 1092-94, (3 March 1997)
	Kohyama, Y., et al., "Buried Bit-Line Cell for 64MB DRAMs", <u>1990 Symposium on VLSI Technology, Digest of Technical Papers</u> , Honolulu, HI, 17-18, (June 4-7, 1990)
	Koshida, N., et al., "Efficient Visible Photoluminescence from Porous Silicon", <u>Japanese Journal of Applied Physics</u> , 30, L1221- L1223, (July 1991)
	Kuge, S., et al., "SOI-DRAM Circuit Technologies for Low Power High Speed Multigiga Scale Memories", <u>IEEE Journal of Solid-State Circuits</u> , 31(4), pp. 586-591, (April 1996)
	Lantz, II, L., "Soft Errors Induced By Alpha Particles", <u>IEEE Transactions on Reliability</u> , 45, 174-179, (June 1996)
	Lehmann, et al., "A Novel Capacitor Technology Based on Porous Silicon", <u>Thin Solid Films</u> 276, Elsevier Science, 138-42, (1996)
	Lehmann, V., "The Physics of Macropore Formation in Low Doped n-Type Silicon", <u>Journal of the Electrochemical Society</u> , 140(10), 2836-2843, (Oct. 1993)

Examiner	Date Considered
----------	-----------------

*Substitute Disclosure Statement Form (PTO-1449)

**EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form 1449*	Atty. Docket No.: 303.389US2	Serial No. Unknown
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	Applicant: Leonard Forbes et al.	
	Filing Date: Herewith	Group: Unknown

OTHER DOCUMENTS

**Examiner
Initial

(Including Author, Title, Date, Pertinent Pages, Etc.)

	Lu, N., et al., "The SPT Cell -- A New Substrate-Plate Trench Cell for DRAMs", <u>1985 IEEE International Electron Devices Meeting, Technical Digest</u> , Washington, D.C., 771-772, (Dec. 1-4, 1985)
	MacSweeney, D., et al., "Modelling of Lateral Bipolar Devices in a CMOS Process", <u>IEEE Bipolar Circuits and Technology Meeting</u> , Minneapolis, MN, 27-30, (Sep. 1996)
	Maeda, S., et al., "A Vertical Phi-Shape Transistor (VPhiT) Cell for 1 Gbit DRAM and Beyond", <u>1994 Symposium of VLSI Technology, Digest of Technical Papers</u> , Honolulu, HI, 133-134, (June 7-9, 1994)
	Maeda, S., et al., "Impact of a Vertical Phi-Shape Transistor (VPhiT) Cell for 1 Gbit DRAM and Beyond", <u>IEEE Transactions on Electron Devices</u> , 42, 2117-2123, (Dec. 1995)
	Malaviya, S., <u>IBM TBD</u> , 15, p. 42, (July 1972)
	Masu, K., et al., "Multilevel Metallization Based on Al CVD", <u>1996 IEEE Symposium on VLSI Technology, Digest of Technical Papers</u> , Honolulu, HI, 44-45, (June 11-13, 1996)
	McCredie, B.D., et al., "Modeling, Measurement, and Simulation of Simultaneous Switching Noise", <u>IEEE Transactions on Components, Packaging, and Manufacturing Technology -- Part B</u> , 19, 461-472, (Aug. 1996)
	Muller, K., et al., "Trench Storage Node Technology for Gigabit DRAM Generations", <u>Digest IEEE International Electron Devices Meeting</u> , San Francisco, CA, 507-510, (Dec. 1996)
	Nitayama, A., et al., "High Speed and Compact CMOS Circuits with Multipillar Surrounding Gate Transistors", <u>IEEE Transactions on Electron Devices</u> , 36, 2605-2606, (Nov. 1989)
	Ohba, T., et al., "Evaluation on Selective Deposition of CVD W Films by Measurement of Surface Temperature", <u>In: Tungsten and Other Refractory Metals for VLSI Applications II</u> , Materials Research Society, Pittsburgh, PA, 59-66, (1987)

Examiner	Date Considered
----------	-----------------

*Substitute Disclosure Statement Form (PTO-1449)

**EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form 1449*	Atty. Docket No.: 303.389US2	Serial No. Unknown
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	Applicant: Leonard Forbes et al.	
	Filing Date: Herewith	Group: Unknown

OTHER DOCUMENTS

**Examiner
Initial

(Including Author, Title, Date, Pertinent Pages, Etc.)

	Okba, T., et al., "Selective Chemical Vapor Deposition of Tungsten Using Silane and Polysilane Reductions", <u>In: Tungsten and Other Refractory Metals for VLSI Applications IV</u> , Materials Research Society, Pittsburgh, PA, 17-25, (1989)
	Ohno, Y., et al., "Estimation of the Charge Collection for the Soft-Error Immunity by the 3D-Device Simulation and the Quantitative Investigation", <u>Simulation of Semiconductor Devices and Processes</u> , 6, 302-305, (Sep. 1995)
	Oowaki, Y., et al., "New alpha-Particle Induced Soft Error Mechanism in a Three Dimensional Capacitor Cell", <u>IEICE Transactions on Electronics</u> , 78-C, 845-851, (July 1995)
	Oshida, S., et al., "Minority Carrier Collection in 256 M-bit DRAM Cell on Incidence of Alpha-Particle Analyzed by Three-Dimensional Device Simulation", <u>IEICE Transactions on Electronics</u> , 76-C, 1604-1610, (Nov. 1993)
	Ott, A.W., et al., "Al3O3 Thin Film Growth on Si(100) Using Binary Reaction Sequence Chemistry", <u>Thin Solid Films</u> , Vol. 292, 135-44, (1997)
	Ozaki, T., et al., "A Surrounding Isolation-Merged Plate Electrode (SIMPLE) Cell with Checkered Layout for 256Mbit DRAMs and Beyond", <u>1991 IEEE International Electron Devices Meeting</u> , Washington, D.C., 469-472, (Dec. 8-11, 1991)
	Parke, S.A., et al., "A High-Performance Lateral Bipolar Transistor Fabricated on SIMOX", <u>IEEE Electron Device Letters</u> , 14, 33-35, (Jan. 1993)
	Pein, H., et al., "A 3-D Sidewall Flash EPROM Cell and Memory Array", <u>IEEE Transactions on Electron Devices</u> , 40, 2126-2127, (Nov. 1993)
	Pein, H., et al., "Performance of the 3-D PENCIL Flash EPROM Cell and Memory Array", <u>IEEE Transactions on Electron Devices</u> , 42, 1982-1991, (November, 1995)
	Pein, H.B., et al., "Performance of the 3-D Sidewall Flash EPROM Cell", <u>IEEE International Electron Devices Meeting, Technical Digest</u> , 11-14, (1993)
GL	Ramo, S., et al., "Fields and Waves in Communication Electronics", <u>John Wiley & Sons, Inc., New York, 3rd ed.</u> , 428-433, (1994)

Examiner

Date Considered

*Substitute Disclosure Statement Form (PTO-1449)

**EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form 1449*	Atty. Docket No.: 303.389US2	Serial No. Unknown
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	Applicant: Leonard Forbes et al.	
	Filing Date: Herewith	Group: Unknown

OTHER DOCUMENTS

**Examiner
Initial

(Including Author, Title, Date, Pertinent Pages, Etc.)

	Rao, K.V., et al., "Trench Capacitor Design Issues in VLSI DRAM Cells", 1986 <u>IEEE International Electron Devices Meeting, Technical Digest</u> , Los Angeles, CA, 140-143, (Dec. 7-10, 1986)
	Richardson, W.F., et al., "A Trench Transistor Cross-Point DRAM Cell", <u>IEEE International Electron Devices Meeting</u> , Washington, D.C., 714-717, (Dec. 1-4, 1985)
	Sagara, K., et al., "A 0.72 micro-meter ² Recessed STC (RSTC) Technology for 256Mbit DRAMs using Quarter-Micron Phase-Shift Lithography", 1992 <u>Symposium on VLSI Technology, Digest of Technical Papers</u> , Seattle, WA, 10-11, (June 2-4, 1992)
	Saito, M., et al., "Technique for Controlling Effective V _{th} in Multi-Gbit DRAM Sense Amplifier", 1996 <u>Symposium on VLSI Circuits, Digest of Technical Papers</u> , Honolulu, HI, 106-107, (June 13-15, 1996)
	Senthinathan, R., et al., "Reference Plane Parasitics Modeling and Their Contribution to the Power and Ground Path "Effective" Inductance as Seen by the Output Drivers", <u>IEEE Transactions on Microwave Theory and Techniques</u> , 42, 1765-1773, (Sep. 1994)
	Shah, A.H., et al., "A 4-Mbit DRAM with Trench-Transistor Cell", <u>IEEE Journal of Solid-State Circuits</u> , SC-21, 618-625, (Oct. 1986)
	Shah, A.H., et al., "A 4Mb DRAM with Cross-Point Trench Transistor Cell", 1986 <u>IEEE International Solid-State Circuits Conference, Digest of Technical Papers</u> , 268-269, (Feb. 21, 1986)
	Sherony, M.J., et al., "Reduction of Threshold Voltage Sensitivity in SOI MOSFET's", <u>IEEE Electron Device Letters</u> , 16, 100-102, (Mar. 1995)
	Shimomura, K., et al., "A 1V 46ns 16Mb SOI-DRAM with Body Control Technique", 1997 <u>IEEE International Solid-State Circuits Conference, Digest of Technical Papers</u> , 68-69, (Feb. 6, 1997)
	Stanisic, B.R., et al., "Addressing Noise Decoupling in Mixed-Signal IC's: Power Distribution Design and Cell Customization", <u>IEEE Journal of Solid-State Circuits</u> , 30, 321-326, (Mar. 1995)

Examiner	Date Considered
----------	-----------------

*Substitute Disclosure Statement Form (PTO-1449)

**EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form 1449*	Atty. Docket No.: 303.389US2	Serial No. Unknown
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	Applicant: Leonard Forbes et al.	
	Filing Date: Herewith	Group: Unknown

OTHER DOCUMENTS

**Examiner
Initial

(Including Author, Title, Date, Pertinent Pages, Etc.)

	Stellwag, T.B., et al., "A Vertically-Integrated GaAs Bipolar DRAM Cell", <u>IEEE Transactions on Electron Devices</u> , 38, 2704-2705, (Dec. 1991)
	Suma, K., et al., "An SOI-DRAM with Wide Operating Voltage Range by CMOS/SIMOX Technology", <u>IEEE Journal of Solid-State Circuits</u> , 29(11), pp. 1323-1329, (November 1994)
	Sunouchi, K., et al., "A Surrounding Gate Transistor (SGT) Cell for 64/256Mbit DRAMs", <u>1989 IEEE International Electron Devices Meeting, Technical Digest</u> , Washington, D.C., 23-26, (Dec. 3-6, 1989)
	Sunouchi, K., et al., "Process Integration for 64M DRAM Using an Asymmetrical Stacked Trench Capacitor (AST) Cell", <u>1990 IEEE International Electron Devices Meeting</u> , San Francisco, CA, 647-650, (Dec. 9-12, 1990)
	Suntola, T., "Atomic Layer Epitaxy", <u>Handbook of Crystal Growth 3, Thin Films of Epitaxy, Part B: Growth Mechanics and Dynamics</u> , Elsevier, Amsterdam, 601-63, (1994)
	Sze, S.M., <u>VLSI Technology</u> , 2nd Edition, Mc Graw-Hill, NY, 90, (1988)
	Takai, M., et al., "Direct Measurement and Improvement of Local Soft Error Susceptibility in Dynamic Random Access Memories", <u>Nuclear Instruments & Methods in Physics Research, B-99</u> , Proceedings of the 13th International Conference on the Application of Accelerators in Research and Industry, Denton, TX, 562-565, (Nov. 7-10, 1994)
	Takato, H., et al., "High Performance CMOS Surrounding Gate Transistor (SGT) for Ultra High Density LSIs", <u>IEEE International Electron Devices Meeting, Technical Digest</u> , 222-225, (1988)
	Takato, H., et al., "Impact of Surrounding Gate Transistor (SGT) for Ultra-High Density LSI's", <u>IEEE Transactions on Electron Devices</u> , 38, 573-578, (Mar. 1991)
	Tanabe, N., et al., "A Ferroelectric Capacitor Over Bit-Line (F-COB) Cell for High Density Nonvolatile Ferroelectric Memories", <u>1995 Symposium on VLSI Technology, Digest of Technical Papers</u> , Kyoto, Japan, 123-124, (June 6-8, 1995)

Examiner

Date Considered

*Substitute Disclosure Statement Form (PTO-1449)

**EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form 1449*	Atty. Docket No.: 303.389US2	Serial No. Unknown
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	Applicant: Leonard Forbes et al.	
	Filing Date: Herewith	Group: Unknown

OTHER DOCUMENTS

**Examiner
Initial

(Including Author, Title, Date, Pertinent Pages, Etc.)

	Temmler, D., "Multilayer Vertical Stacked Capacitors (MVSTC) for 64Mbit and 256Mbit DRAMs", <u>1991 Symposium on VLSI Technology, Digest of Technical Papers</u> , Oiso, 13-14, (May 28-30, 1991)
	Terauchi, M., et al., "A Surrounding Gate Transistor (SGT) Gain Cell for Ultra High Density DRAMs", <u>1993 Symposium on VLSI Technology, Digest of Technical Papers</u> , Kyoto, Japan, 21-22, (1993)
	Tsui, P.G., et al., "A Versatile Half-Micron Complementary BiCMOS Technology for Microprocessor-Based Smart Power Applications", <u>IEEE Transactions on Electron Devices</u> , 42, 564-570, (Mar. 1995)
	Verdonckt-Vandebroek, S., et al., "High-Gain Lateral Bipolar Action in a MOSFET Structure", <u>IEEE Transactions on Electron Devices</u> 38, 2487-2496, (Nov. 1991)
	Vittal, A., et al., "Clock Skew Optimization for Ground Bounce Control", <u>1996 IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers</u> , San Jose, CA, 395-399, (Nov. 10-14, 1996)
	Wang, N., <u>Digital MOS Integrated Circuits</u> , Prentice Hall, Inc., Englewood Cliffs, NJ, p. 328-333, (1989)
	Wang, P.W., et al., "Excellent Emission Characteristics of Tunneling Oxides Formed Using Ultrathin Silicon Films for Flash Memory Devices", <u>Japanese Journal of Applied Physics</u> , 35, 3369-3373, (June 1996)
	Watanabe, H., et al., "A New Cylindrical Capacitor Using Hemispherical Grained Si (HSG-Si) for 256Mb DRAMs", <u>IEEE International Electron Devices Meeting, Technical Digest</u> , San Francisco, CA, 259-262, (Dec. 13-16, 1992)
	Watanabe, H., et al., "A Novel Stacked Capacitor with Porous-Si Electrodes for High Density DRAMs", <u>1993 Symposium on VLSI Technology, Digest of Technical Papers</u> , Kyoto, Japan, 17-18, (1993)
	Watanabe, H., et al., "An Advanced Fabrication Technology of Hemispherical Grained (HSG) Poly-Si for High Capacitance Storage Electrodes", <u>Extended Abstracts of the 1991 International Conference on Solid State Devices and Materials</u> , Yokohama, Japan, 478-480, (1991)

Examiner	Date Considered
----------	-----------------

*Substitute Disclosure Statement Form (PTO-1449)

**EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form 1449*	Atty. Docket No.: 303.389US2	Serial No. Unknown
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	Applicant: Leonard Forbes et al.	
	Filing Date: Herewith	Group: Unknown

OTHER DOCUMENTS

**Examiner
Initial

(Including Author, Title, Date, Pertinent Pages, Etc.)

	Watanabe, H., et al., "Device Application and Structure Observation for Hemispherical-Grained Si", <u>J. Appl. Phys.</u> , 71, 3538-3543, (Apr. 1992)
	Watanabe, H., et al., "Hemispherical Grained Silicon (HSG-Si) Formation on In-Situ Phosphorous Doped Amorphous-Si Using the Seeding Method", <u>Extended Abstracts of the 1992 International Conference on Solid State Devices and Materials</u> , Tsukuba, Japan, 422-424, (1992)
	Watanabe, S., et al., "A Novel Circuit Technology with Surrounding Gate Transistors (SGT's) for Ultra High Density DRAM's", <u>IEEE Journal of Solid-State Circuits</u> , 30, 960-971, (Sep. 1995)
	Wooley, et al., "Experimental Results and Modeling Techniques for Substrate Noise in Mixed Signal Integrated Circuits", <u>IEEE Journal of Solid State Circuits</u> , Vol SC-28, 420-30, (1993)
	Yamada, T., et al., "A New Cell Structure with a Spread Source/Drain (SSD) MOSFET and a Cylindrical Capacitor for 64-Mb DRAM's", <u>IEEE Transactions on Electron Devices</u> , 38, 2481-2486, (Nov. 1991)
	Yamada, T., et al., "Spread Source/Drain (SSD) MOSFET Using Selective Silicon Growth for 64Mbit DRAMs", <u>1989 IEEE International Electron Devices Meeting, Technical Digest</u> , Washington, D.C., 35-38, (Dec. 3-6, 1989)
	Yoshikawa, K., "Impact of Cell Threshold Voltage Distribution in the Array of Flash Memories on Scaled and Multilevel Flash Cell Design", <u>1996 Symposium on VLSI Technology, Digest of Technical Papers</u> , Honolulu, HI, 240-241, (June 11-13, 1996)

Examiner	Date Considered
----------	-----------------

*Substitute Disclosure Statement Form (PTO-1449)

**EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.